COMP2611: Computer Organization

Introduction to
Combinational Logic and Sequential Logic

An Exercise On Using Boolean Algebra

- **Show that**

$$A + \overline{A}B = A + B$$

- Solution:

A + ~AB = A1 + ~AB (Identity law)

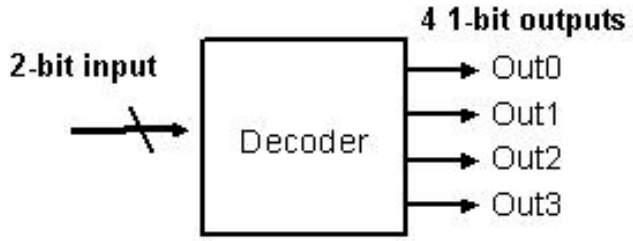
=A(1+B) + ~AB (Annihilator law, zero and one)

= A + AB + ~AB (Distributivity law)

= A + B(A+~A) (Distributivity law)

=A + B (complement law)

Question 1: A decoder takes a single N-bit input and outputs 2^N 1-bit signals. The 1-bit output corresponds to the N-bit input bit pattern is true while all other outputs are false. The following figure shows a block diagram for a 2-to-4 decoder.



A 2-bit decoder

Exercises

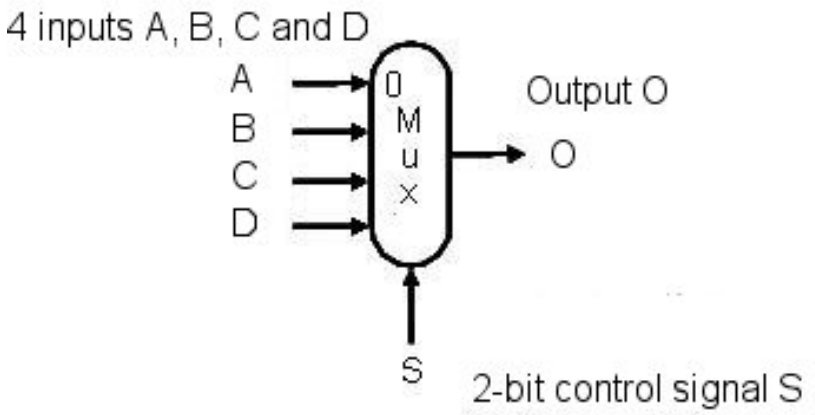
- Why a 2-bit input can generate 4 outputs in the decoder?
  because 2 bit will give a total of 2^2=4 different combination. Therefore up to 4 outputs can be generated
- If the input bits are 11, what will happen to the outputs of the decoder?

  '11' corresponds to 3, therefore Out3 will carry the signal '1' while all the other outputs carry the signal '0'. The decoder effectively 'decodes' the 2-bit binary number '11' and asserts the corresponding output line.
- Is it possible to have more than one outputs asserted? No
- Name two potential uses of the decoder.

  row/column selection in memory referencing, instruction decoding, etc

- Implement the decoder using Logisim

Question 2: A multiplexor is a devices that given the control signal, selects one of the inputs to be forwarded to the output. The following figure shows a 4-input multiplexor.



Exercises

- If the inputs A/B are 32-bit in width, what is the data width of the Output O? 32-bit

- What is the maximum number of inputs if the control signal is 10-bit in width? 2^10 = 1024

- What is the bit-width of the control signal for the multiplexor if there are 9 inputs? ceil($\log_2 9$) = ceil(3.17) = 4-bit