COMP2611: Computer Organization

Cache

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Exercises

Question 1: Consider a single-level cache. For every 100 references to the memory by the CPU, 10 of them are cache misses. A hit in the cache takes 2 clock cycles, and the miss penalty (i.e., access to the RAM) is 10 clock cycles.

(a) What is the hit rate for the cache?

(b) What is the average memory access time per instruction for this cache system?

Question 2: Consider a two level cache hierarchy (i.e., with cache level 1 and cache level 2). For all the references to the memory by the CPU, 20% of them are misses in only level 1 cache. 5% of them are misses in both level 1 and level 2 caches. A hit in level 1 cache takes 1 clock cycle, a hit in level 2 takes 10 clock cycles, and the miss penalty of level 2 (i.e., access to the RAM) is 100 clock cycles.

(a) What is the local miss rate for level 1 cache and for level 2 cache?

(b) What is the average memory access time per instruction for this cache system?

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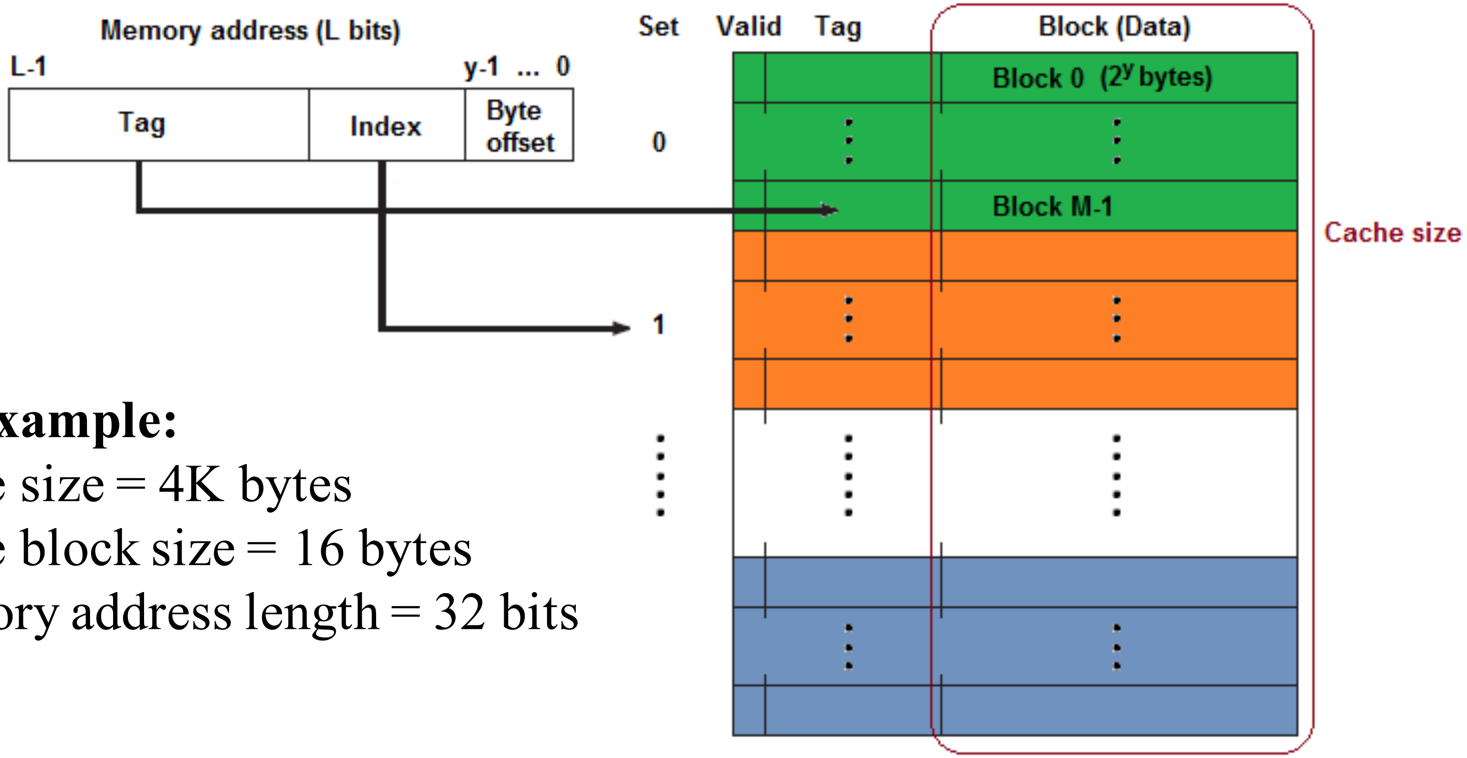
M-way set associative cache



For example:
Cache size = 4K bytes
Cache block size = 16 bytes
Memory address length = 32 bits

Number of blocks in cache = Cache size / Cache block size

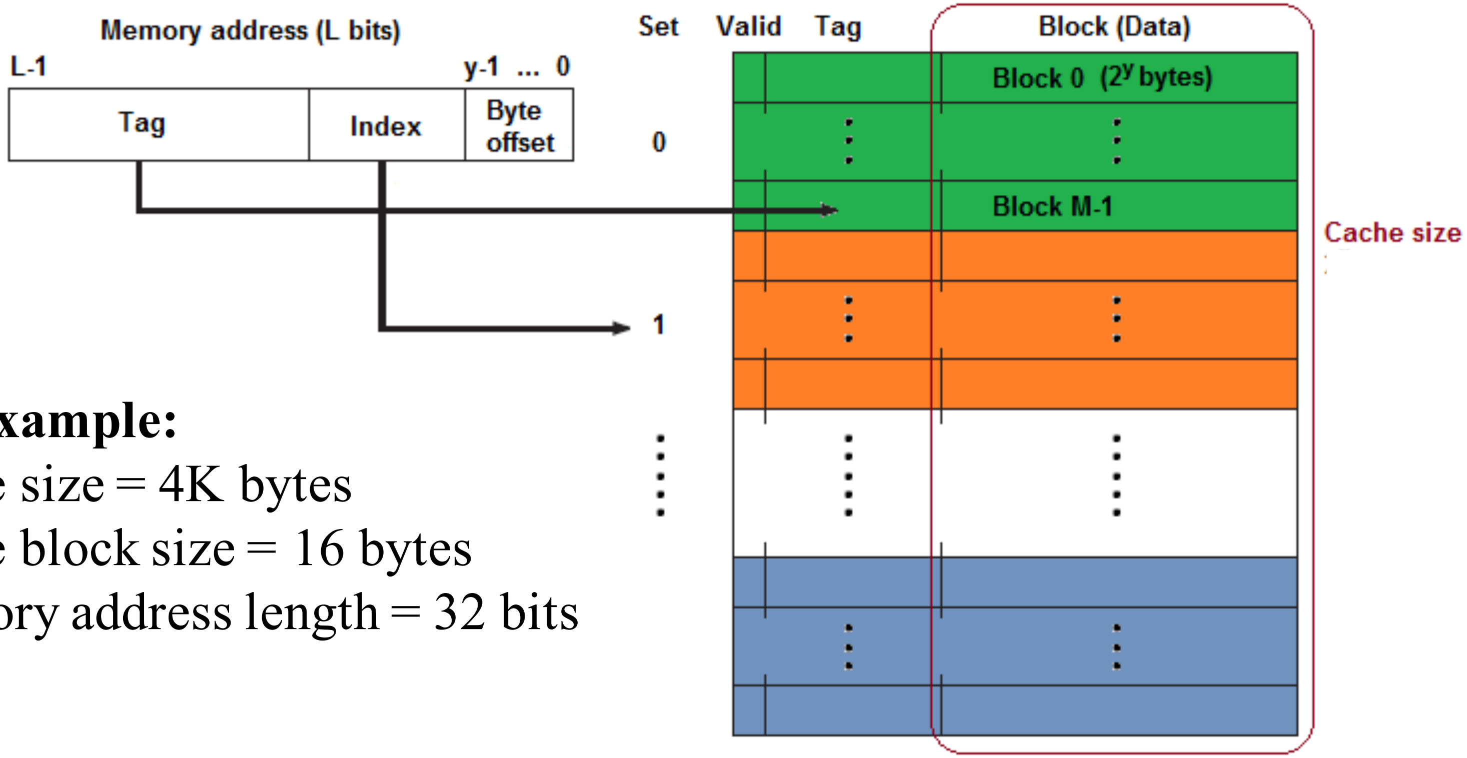
Number of sets in cache = Number of blocks in cache / M = 2^s

Number of bits for Byte offset = y

Number of bits for Index field = s (for 2^s sets in cache)

Number of bits for Tag field = L - s - y (for L-bit address)

M-way set associative cache



For example:
Cache size = 4K bytes
Cache block size = 16 bytes
Memory address length = 32 bits

Total bits required for the cache = (Number of entries) x (size of an entry) = (Number of blocks) x (Cache block size + size of Tag + one valid bit)

Cache size information

- A direct-mapped cache can be treated as a M-way set associative cache with M = 1.
- A fully-associative cache can also be treated as a M-way set associative cache with M = the number of blocks in the cache.
    - Number of blocks in cache = Cache size / Cache block size

Exercises

Question 1: Consider a direct-mapped cache with:

Cache size = 4K bytes

Cache block size = 16 bytes

Memory address length = 32 bits

(a) Complete the following information about the cache?

Cache associativity = 1

Number of blocks in cache =

Number of sets in cache =

Number of bits for Byte offset =

Number of bits for Index field =

Number of bits for Tag field =

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(b) How many bits in total are required for the cache?

Exercises

Question 2: Consider a 4-way set associative cache with:

Cache size = 4K bytes

Cache block size = 16 bytes

Cache associativity = 4

Memory address length = 32 bits

(a) Complete the following information about the cache?

Number of blocks in cache =

Number of sets in cache =

Number of bits for Byte offset =

Number of bits for Index field =

Number of bits for Tag field =

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(b) How many total bits are required for the cache?

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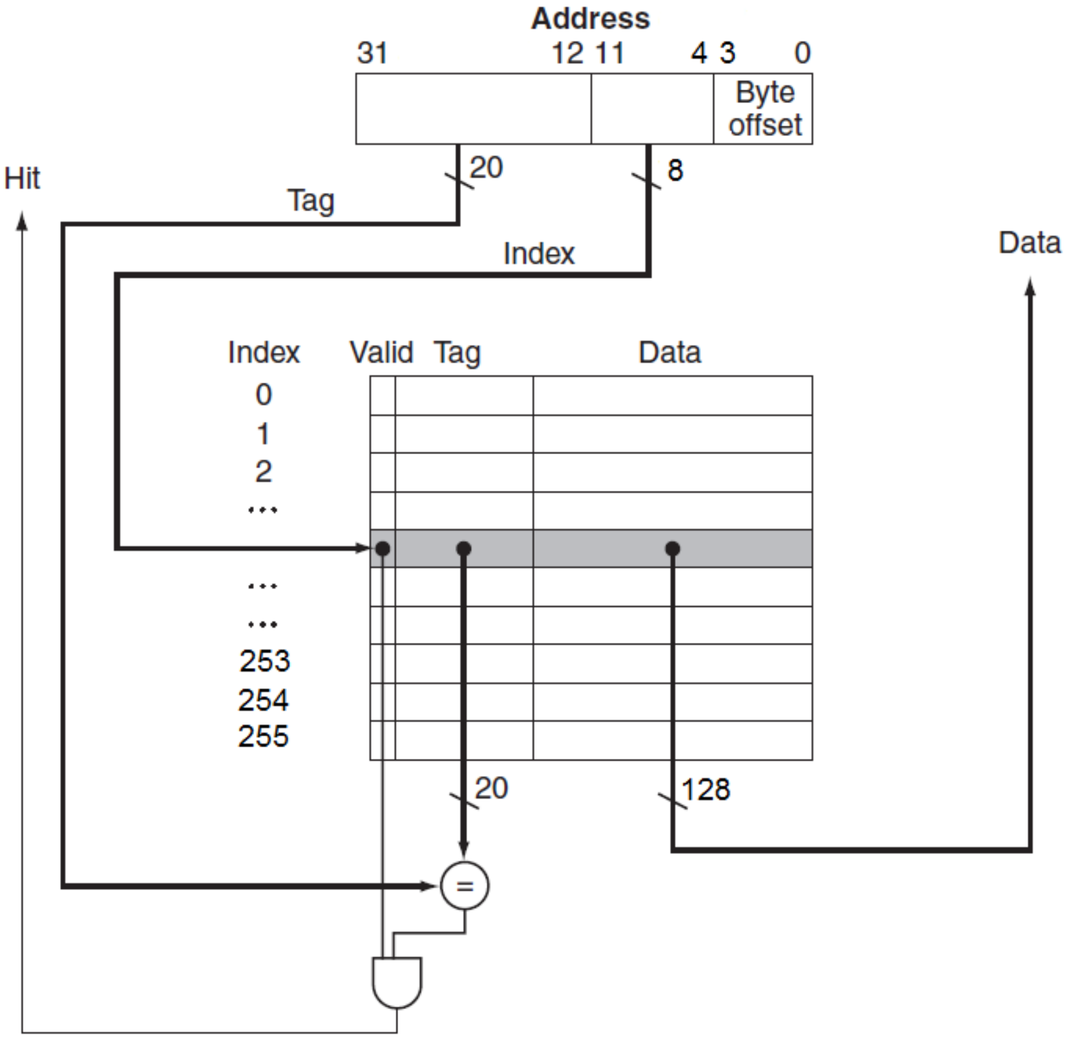
Question 1: Consider the following direct-mapped cache:



Exercises

Complete the last two columns of the following table for the given sequence of memory accesses:

Address of the memory access generated by CPU		Assigned cache set	Hit or miss in cache
0x00123456	0000 0000 0001 0010 0011 0100 0101 0110		
0x00144680	0000 0000 0001 0100 0100 0110 1000 0000		
0x00143458	0000 0000 0001 0100 0011 0100 0101 1000		
0x00143456	0000 0000 0001 0100 0011 0100 0101 0110		
0x00123457	0000 0000 0001 0010 0011 0100 0101 0111		
0x0014445A	0000 0000 0001 0100 0100 0100 0101 1010		

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Exercises

Question 1: Consider the 4-way set associative cache with a 3-bit Tag field and the LRU block replacement policy. A sequence of memory accesses that all map to the same cache set is given in the following table. Complete the table with the current blocks in the set and the cache hits or misses.

	Tag field of the memory accesses generated by CPU (from left to right)							
	010	111	001	010	001	101	110	110
MRU								
LRU								
Hit or miss								

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Question 1: Consider a three level cache hierarchy (i.e., with cache levels 1, 2 and 3). For all the references to the memory by the CPU, 20% of them are misses in only level 1 cache. 10% of them are misses in both level 1 and level 2 caches. 6% of them are misses in all the three levels. A hit in level 1 cache takes 1 clock cycle, a hit in level 2 takes 10 clock cycles, a hit in level 3 takes 20 cycles and the miss penalty of level 3 is 100 clock cycles.

(a) What is the local miss rate for level 2 cache and for level 3 cache?

(b) What is the average memory access time per instruction for this cache system?

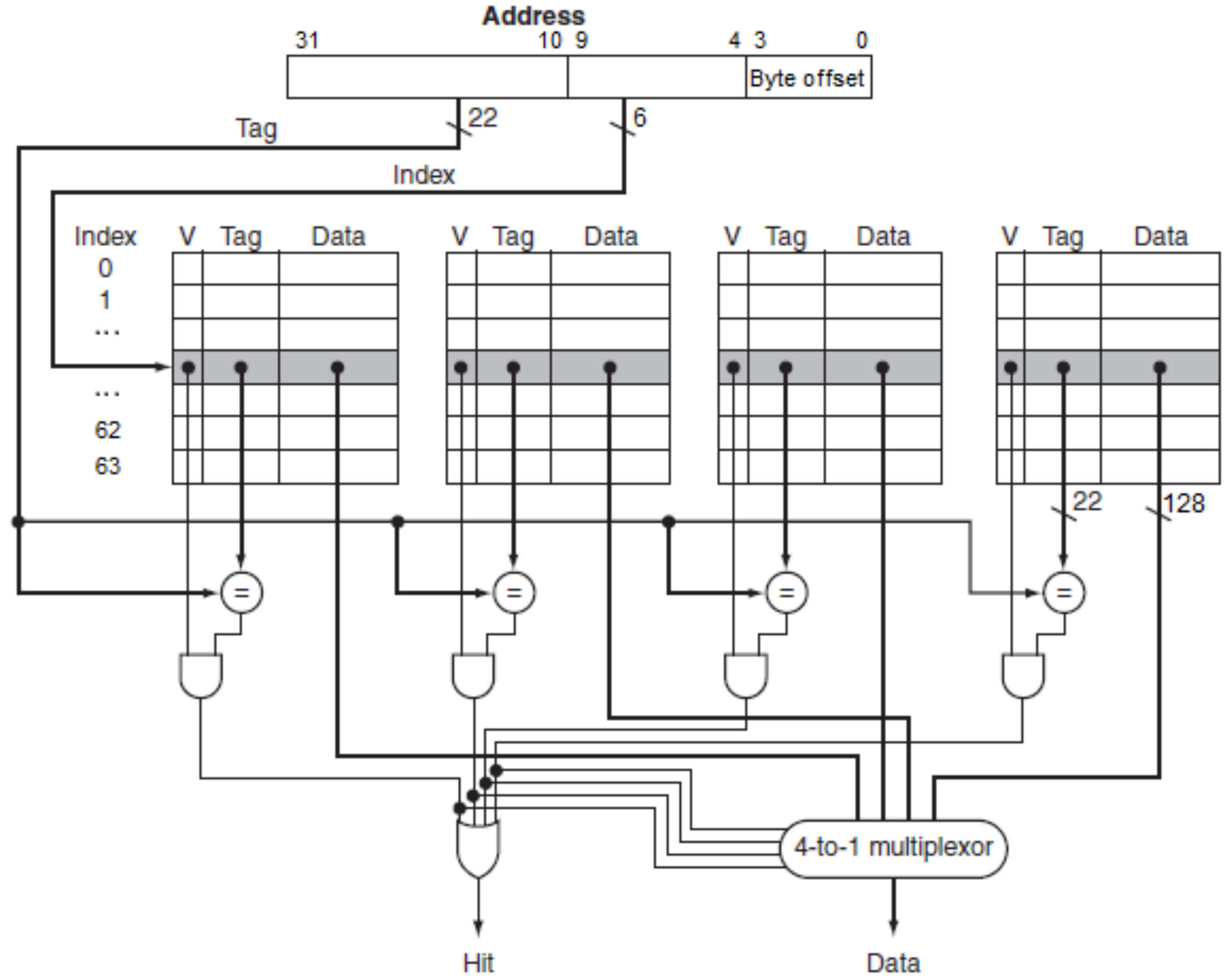
Exercises

Question 2: Consider a two level cache hierarchy (i.e., with cache level 1 and cache level 2). For every 100 references to the memory by the CPU, there are 40 misses in level 1 cache and 20 misses in level 2 cache. A hit in level 1 cache takes 1 clock cycle, a hit in level 2 takes 10 clock cycles, and the miss penalty of level 2 (i.e., access to the RAM) is 100 clock cycles.

(a) What is the local miss rate for level 1 cache and for level 2 cache?

(b) What is the average memory access time per instruction for this cache system?

Question 3: Consider the following 4-way set associative cache:



Exercises

Complete the last two columns of the following table for the given sequence of memory accesses:

Address of the memory access generated by CPU		Assigned cache set	Hit or miss in cache
0x00123456	0000 0000 0001 0010 0011 0100 0101 0110		
0x00144680	0000 0000 0001 0100 0100 0110 1000 0000		
0x00143458	0000 0000 0001 0100 0011 0100 0101 1000		
0x00143456	0000 0000 0001 0100 0011 0100 0101 0110		
0x00123457	0000 0000 0001 0010 0011 0100 0101 0111		
0x0014445A	0000 0000 0001 0100 0100 0100 0101 1010		